NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. R2184.045/P045

Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

POWER CONTROL APPARATUS FOR A BATTERY-POWERED COMMUNICATION SYSTEM

and invented by:

Tatsuya Fujii

If a CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 34 pages(s) and including the following:
   - a. [X] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [X] Background of the invention
   - f. [X] Brief summary of the invention
   - g. [X] Brief description of the drawings *(if drawings filed)*
   - h. [X] Detailed description
   - i. [X] Claims as classified below
   - j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [X] Formal [ ] Informal Number of sheets: 6

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [X] With Power of Attorney [ ] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [ ] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [X] Information Disclosure Statement/PTO-1449 [X] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [X] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	11	- 20 =		x $18.00	
Independent Claims	2	- 3 =		x $78.00	
Multiple Dependent Claims (check if applicable)			☐		
Other Fees (specify purpose): Recordation Assignment					$40.00
				BASIC FEE	$800.00
				TOTAL FILING FEE	$800.00

☒ A check in the amount of $800.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: March 8, 1999

Mark J. Thronson
Attorney Reg. No.: 33,082
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, NW
Washington, DC 20037-1526
(202) 785-9700

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, TATSUYA FUJII, a citizen of Japan residing at Kanagawa, Japan have invented certain new and useful improvements in

POWER CONTROL APPARATUS FOR A BATTERY-POWERED COMMUNICATION SYSTEM

of which the following is a specification:-

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a power control apparatus which is suitable for use in a battery-powered system, such as a cellular mobile telephone or a portable electronic device.

(2) Description of the Related Art

A power control apparatus provided in a battery-powered system, such as a cellular mobile telephone or a portable electronic device, is known. In the power control apparatus, a source voltage of a battery is converted into a controlled voltage, and the controlled voltage is supplied to each of driven circuits (or functional elements) of the system. There is a demand for the power control apparatus of this type to reduce a power consumption of the driven circuits. In recent years, the power control apparatus of this type has been improved for the purpose of reducing a power consumption of the driven circuits.

For example, Japanese Laid-Open Patent Application No. 5-088790 discloses a power control system which is adapted to allow a sleep-mode operation of a CPU (central processing unit) in which the operation of the CPU is assured and the power of the CPU is turned OFF.

Japanese Laid-Open Patent Application No.

5-265597 discloses a micro-controller which allows a driven circuit to operate at a low voltage in a selected mode. In the micro-controller, a source voltage supplied to the driven circuit is controlled so as to meet one of power consumption reduction, operating speed increase and noise reduction modes.

Japanese Laid-Open Patent Application No. 6-139373 discloses a semiconductor device provided with a switch selectable between a normal power mode and a power saving mode. In the semiconductor device, a voltage supplied to a driven circuit is controlled by setting the switch to select one of the two modes.

FIG. 7 shows a conventional power control apparatus. The conventional power control apparatus of FIG. 7 includes a power-supply circuit 61 which supplies a source voltage of a first battery 60a through a diode 80 to a driven circuit 71. A power-supply circuit 62 supplies the source voltage of the first battery 60a to each of a driven circuit 72 and a power-supply circuit 63. The power-supply circuit 63 supplies a lower voltage, derived from the source voltage of the first battery 60a or from the power-supply circuit 62, to a driven circuit 73. A source voltage of a second battery 60b is supplied through a diode 81 to the driven circuit 71.

In the conventional power control apparatus

of FIG. 7, the second battery 60b and the diode 81 constitute a backup power supply that acts to supply the source voltage of the second battery 60b to the driven circuit 71 when the source voltage of the first battery 60a supplied to the driven circuit 71 by the power-supply circuit 61 is discontinued. The power-supply circuit 63 acts as a dependent circuit that operates in dependence on a power-supply operation of the power-supply circuit 62. That is, the dependent power-supply circuit 63 operates to supply the lower voltage to the driven circuit 73 when the power-supply circuit 62 is operating. The dependent power-supply circuit 63 may include a DC-DC converter or a voltage regulator.

The relationship between the power-supply circuit 62 and the dependent power-supply circuit 63 is needed when the conventional power control apparatus includes functional blocks indicated by a dotted line in FIG. 7. That is, the relationship between the power-supply circuit 62 and the dependent power-supply circuit 63 is needed when one of the functional blocks (for example, the driven circuit 72) is driven by the power-supply circuit 72 at the source voltage of the battery 60a while the other functional block (for example, the driven circuit 73) is driven by the power-supply circuit 63 at the lower voltage derived from the source voltage.

In the conventional power control apparatus of FIG. 7, each of the driven circuits 71, 72 and 73 is provided with an oscillation circuit. When the oscillation circuit generates a clock signal with a lowered frequency and supplies the clock signal to the driven circuit of concern, the driven circuit is set in a low-speed mode so that it operates at a low speed. When the oscillation circuit stops supplying the clock signal, the driven circuit of concern is set in a stand-by mode. By using the oscillation circuits of the driven circuits 71, 72 and 73, the conventional power control apparatus of FIG. 7 acts to reduce the power consumption of the driven circuits 71, 72 and 73.

In the conventional power control apparatus of FIG. 7, if the source voltage is continuously supplied to the driven circuit of concern during the stand-by mode, it is difficult to completely prevent the flow of a leak current from a MOS (metal oxide semiconductor) transistor of the driven circuit. In order to eliminate this problem, it is necessary for the power-supply circuits 61 and 62 to stop the supplying of the source voltage of the first battery 60a to the driven circuits 71 and 72 when the driven circuit is in the stand-by mode.

However, in the conventional power control apparatus of FIG. 7, the power-supply circuit 63 continues

to supply the lower voltage to the driven circuit 73 during the operation of the power-supply circuit 62. Even when the operation of the driven circuit 73 is not needed, the power-supply circuit 63 continuously supplies the lower voltage to the driven circuit 73. In such a condition, the driven circuit 73 unnecessarily consumes the power supplied by the power-supply circuit 63, and the conventional power control apparatus of FIG. 7 does not act to reduce the power consumption of the driven circuit 73.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved power control apparatus in which the above-described problems are eliminated.

Another object of the present invention is to provide a power control apparatus which is effective in reducing a power consumption of a driven circuit by suitably controlling a power-supply operation of a secondary power-supply circuit which supplies power to the driven circuit in dependence on a power-supply operation of a primary power-supply circuit.

The above-mentioned objects of the present invention are achieved by a power control apparatus including: a first driven circuit; a second driven circuit

which is connected to the first driven circuit; a primary power-supply circuit which produces a primary voltage from a source voltage of a battery and supplies the primary voltage to drive the first driven circuit; a secondary power-supply circuit which produces a secondary voltage from the source voltage of the battery or from the primary voltage of the primary power-supply circuit and supplies the secondary voltage to drive the second driven circuit; and a control circuit which outputs a power-supply control signal to the secondary power-supply circuit in response to a command signal, so that the supply of the secondary voltage to the second driven circuit by the secondary power-supply circuit is started or terminated by the power-supply control signal.

The above-mentioned objects of the present invention are achieved by a power control apparatus including: a first driven circuit; a second driven circuit which is connected to the first driven circuit; a primary power-supply circuit which is connected to a battery, the primary power-supply circuit producing a primary voltage from a source voltage of the battery and supplying the primary voltage to drive the first driven circuit; a secondary power-supply circuit which is connected to the primary power-supply circuit, the secondary power-supply circuit producing a secondary voltage from the source

voltage of the battery or from the primary voltage of the primary power-supply circuit and supplying the secondary voltage to drive the second driven circuit; a primary oscillation part which outputs a clock signal to the first driven circuit; a primary reset generating part which outputs a primary reset signal to the first driven circuit when an oscillation of the primary oscillation part is detected to be stable, the primary reset signal causing the first driven circuit to start operation in accordance with the clock signal output by the primary oscillation part; a control signal generating part, connected to both the first driven circuit and the secondary power-supply circuit, which outputs a power-supply control signal to the secondary power-supply circuit in response to a command signal output by the first driven circuit, so that the supply of the secondary voltage to the second driven circuit by the secondary power-supply circuit is started or terminated by the power-supply control signal; a secondary oscillation part which outputs a clock signal to the second driven circuit; and a secondary reset generating part which outputs a secondary reset signal to the second driven circuit when an oscillation of the secondary oscillation part is detected to be stable, the secondary reset signal causing the second driven circuit to start operation in accordance with the clock signal

output by the secondary oscillation part.

The power control apparatus according to the present invention is effective in reducing the power consumption of the second driven circuit in contrast to the conventional power control apparatus. In a preferred embodiment of the power control apparatus of the present invention, the power-supply operation of the secondary power-supply circuit is suitably controlled such that the supply of the secondary voltage to the second driven circuit is enabled by a high-state power-supply control signal only when it is needed, and the supply of the secondary voltage to the second driven circuit is disabled by a low-state power-supply control signal when it is unneeded. In a preferred embodiment of the power control apparatus of the present invention, the oscillation of the secondary oscillation part is quickly stabilized after a start command signal is output to the control signal generating part by the first driven circuit, and it is possible to achieve a speedy power-supply operation of the first and second driven circuits. Further, a preferred embodiment of the power control apparatus of the present invention acts to prevent the flow of a leak current from the first driven circuit into the second driven circuit when the supply of the secondary voltage to the second driven circuit is stopped, and it is possible to more

effectively reduce the power consumption of the driven circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of a power control apparatus embodying the present invention;

FIG. 2 is a circuit diagram of a control circuit of the power control apparatus of FIG. 1;

FIG. 3 is a time chart for explaining operations of the control circuit of the power control apparatus of FIG. 2;

FIG. 4 is a time chart for explaining power-saved periods during an operation of the power control apparatus of FIG. 1;

FIG. 5 is a circuit diagram of a modification of a secondary oscillation circuit in the control circuit of FIG. 2;

FIG. 6A and FIG. 6B are circuit diagrams of a modification of first and second driven circuits in the power control apparatus of FIG. 1; and

FIG. 7 is a block diagram of a conventional

power control apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given of the preferred embodiments of the present invention with reference to the accompanying drawings.

FIG. 1 shows an embodiment of a power control apparatus of the present invention.

As shown in FIG. 1, the power control apparatus in the present embodiment includes a power-supply circuit 2 which supplies a source voltage of a battery 10 through a diode 4 to a driven circuit 5. A source voltage of a battery 1 is supplied through a diode 3 to the driven circuit 5. The battery 1 and the diode 3 constitute a backup power supply that acts to supply the source voltage of the battery 1 to the driven circuit 5 when the source voltage of the battery 10 supplied to the driven circuit 5 by the power-supply circuit 2 is discontinued.

The elements 1, 2, 3, 4 and 5 of the power control apparatus, shown in FIG. 1, are essentially the same as the elements 60a, 61, 81, 80 and 71 of the conventional power control apparatus of FIG. 7, respectively, and a description thereof will be omitted for the sake of simplicity of description.

In the power control apparatus of FIG. 1, a primary power-supply circuit 11 has an input connected to the battery 10. The battery 10 is, for example, a 5-V battery. A secondary power-supply circuit 12 has an input connected to an output of the primary power-supply circuit 11. The primary power-supply circuit 11 produces a primary voltage (for example, 3 V) from the source voltage of the battery 10, and supplies the primary voltage through a power-supply line 31 to a first driven circuit 21. The secondary power-supply circuit 12 produces a secondary voltage (for example, 2 V) from the source voltage of the battery 10 or from the primary voltage of the primary power-supply circuit 11, and supplies the secondary voltage through a power-supply line 32 to a second driven circuit 22.

The secondary power-supply circuit 12 acts as a dependent circuit that operates in dependence on a power-supply operation of the primary power-supply circuit 11. That is, the dependent power-supply circuit 12 operates to supply the secondary voltage to the second driven circuit 22 when the first power-supply circuit 11 is operating.

The first driven circuit 21 and the second driven circuit 12 are interconnected by a data line 23. A data signal output by the first driven circuit 21 is

received by the second driven circuit 22 through the data line 23, and the second driven circuit 22 processes the received data. A data signal, indicating the processed data, output by the second driven circuit 22 is received by the first driven circuit 21, and the first driven circuit 21 further processes the received data.

The first driven circuit 21 and the second driven circuit 22 do not necessarily start operation at the same time. The first driven circuit 21 may solely start operation when the second driven circuit 22 stops operation. The second driven circuit 22 may not solely start operation when the first driven circuit 21 stops operation. The second driven circuit 22 starts operation only when the first driven circuit 21 is operating.

In the power control apparatus of FIG. 1, a control circuit 13 which includes a voltage detection unit 130 and a secondary power control unit 131 is provided.

FIG. 2 shows a configuration of the control circuit 13 of the power control apparatus of FIG. 1. FIG. 3 is a time chart for explaining operations of the control circuit of FIG. 2. The control circuit 13, including the voltage detection unit 130 and the secondary power control unit 131, is indicated by a dotted line in FIG. 2.

A description will be given of the configuration and operations of the control circuit of the

power control apparatus in the present embodiment with reference to FIG. 2 and FIG. 3.

As indicated by (a) in FIG. 3, after a delay of a given period from a start of operation of the primary power-supply circuit 11, the primary power-supply circuit 11 is set in an operating condition that it can supply the primary voltage (for example, 3 V) to the first driven circuit 21.

The voltage detection unit 130 includes a primary voltage detection part 130a and a secondary voltage detection part 130b as shown in FIG. 2. As indicated by (b) in FIG. 3, the primary voltage detection part 130a detects the primary voltage supplied by the primary power-supply circuit 11 when the primary power-supply circuit 11 is set in the operating condition, and outputs a high-state signal to the secondary power control unit 131 of the control circuit 13.

The secondary power control unit 131 includes a primary oscillation part 133 as shown in FIG. 2. As indicated by (c) in FIG. 3, the primary oscillation part 133 starts oscillation at the same time as the start of operation of the primary power-supply circuit 11. After a delay of a given period, a clock signal (CK) produced by the oscillation of the primary oscillation part 133 becomes stable.

The secondary power control unit 131 includes a primary reset generating part 132, and the primary reset generating part 132 is constructed by two flip-flop circuits which are connected in a manner shown in FIG. 2. As indicated by (d) in FIG. 3, after a delay of a given period since the time the high-state signal is output by the primary voltage detection part 130a, the primary reset generating part 132 outputs a high-state signal (or a primary reset signal) to the first driven circuit 21.

When the primary reset signal output by the primary reset generating part 132 is received, the first driven circuit 21 starts operation. At the start of operation, the stable clock signal (CK) output by the primary oscillation part 133 is supplied to the first driven circuit 21, and the primary voltage output by the primary power-supply circuit 11 is supplied to the first driven circuit 21 through the power-supply line 31. The primary oscillation part 133 and the primary reset generating part 132 are driven by the power supplied from the primary power-supply circuit 11.

The secondary power control unit 131 includes a control signal generating part 136 as shown in FIG. 2. When transmitting the processed data from the first driven circuit 21 to the second driven circuit 22

via the data line 23, the first driven circuit 21 sends a start command signal to the control signal generating part 136. The start command signal causes the control signal generating part 136 to output a power-supply control signal (or a high-state signal) to the secondary power-supply circuit 12. As the secondary power-supply circuit 12 starts supplying the secondary voltage to the second driven circuit 12 in response to the high-state power-supply control signal, the second driven circuit 22 quickly starts operation by the power supplied from the secondary power-supply circuit 12.

As indicated by (e) in FIG. 3, when the start command signal output by the first driven circuit 21 is received, the control signal generating part 136 outputs the power-supply control signal (or the high-state signal) to each of the secondary power-supply circuit 12 and the secondary voltage detection part 130b.

On the other hand, when receiving the processed data from the second driven circuit 22 at the first driven circuit 21 via the data line 23, the first driven circuit 21 sends an end command signal to the control signal generating part 136. The end command signal causes the control signal generating part 136 to output a low-state power-supply control signal to the secondary power-supply circuit 12. As the secondary

power-supply circuit 12 stops supplying the secondary voltage to the second driven circuit 22 in response to the low-state power-supply control signal, the second driven circuit 22 quickly terminates the power-supply operation after the processed data from the second driven circuit 22 is supplied to the first driven circuit 21.

As indicated by (e) in FIG. 3, when the end command signal output by the first driven circuit 21 is received, the control signal generating part 136 outputs the low-state power-supply control signal to each of the secondary power-supply circuit 12 and the secondary voltage detection part 130b.

In the control circuit 13 of FIG. 2, the detection signal output by the primary voltage detection part 130a is supplied through a signal line 24 to the control signal generating part 136. Even when the start command signal output by the first driven circuit 21 is received, the control signal generating part 136 acts to delay the start of operation of the secondary power-supply circuit 12 until a high-state detection signal output by the primary voltage detection part 130a is received. When a low-state detection signal output by the primary voltage detection part 130a is received, the control signal generating part 136 acts to stop the operation of the secondary power-supply circuit 12.

The secondary voltage detection part 130b starts operation when the high-state power-supply control signal output by the control signal generating part 136 is received. Also, the secondary power-supply circuit 12 starts operation when the high-state power-supply control signal is received. As indicated by (f) in FIG. 3, after a delay of a given period from the start of operation, the secondary power-supply circuit 12 is set in an operating condition that it can supply the secondary voltage (for example, 2 V) to the second driven circuit 22.

The secondary power control unit 131 includes a secondary reset generating part 134 and a secondary oscillation part 135 as shown in FIG. 2. As indicated by (g) in FIG. 3, the secondary voltage detection part 130b detects the secondary voltage supplied by the secondary power-supply circuit 12 when the secondary power-supply circuit 12 is set in the operating condition, and outputs a high-state signal to each of the secondary reset generating part 134 and the secondary oscillation part 135 of the secondary power control unit 131.

As indicated by (h) in FIG. 3, the secondary oscillation part 135 starts oscillation at the same time as the start of operation of the secondary power-supply circuit 12. After a delay of a given period,

a clock signal (CK) produced by the oscillation of the secondary oscillation part 135 becomes stable.

The secondary reset generating part 134 of the secondary power control unit 131 is constructed by two flip-flop circuits which are connected in a manner shown in FIG. 2. As indicated by (i) in FIG. 3, after a delay of a given period since the time the high-state signal is output by the secondary voltage detection part 130b, the secondary reset generating part 134 outputs a high-state signal (or a secondary reset signal) to the second driven circuit 22.

When the secondary reset signal output by the secondary reset generating part 134 is received, the second driven circuit 22 starts operation. At the start of operation, the stable clock signal (CK) output by the secondary oscillation part 135 is supplied to the second driven circuit 22, and the secondary voltage output by the secondary power-supply circuit 12 is supplied to the second driven circuit 22 through the power-supply line 32. The secondary oscillation part 135 and the secondary reset generating part 134 are driven by the power supplied from the secondary power-supply circuit 12.

As previously described, in the conventional power control apparatus of FIG. 7, even when the operation of the driven circuit 73 is not needed, the

power-supply circuit 63 continuously supplies the lower voltage to the driven circuit 73. In such a condition, the driven circuit 73 unnecessarily consumes the power supplied by the power-supply circuit 63.

FIG. 4 shows power-saved periods during an operation of the power control apparatus of FIG. 1.

In contrast to the conventional power control apparatus of FIG. 7, the above-described embodiment of the power control apparatus is effective in reducing the power consumption of the second driven circuit 22. As shown in FIG. 4, the power-supply operation of the secondary power-supply circuit 12 is suitably controlled such that the supply of the secondary voltage to the second driven circuit 22 is enabled by the high-state power-supply control signal only when it is needed, and the supply of the secondary voltage to the second driven circuit 22 is disabled by the low-state power-supply control signal when it is unneeded.

In order to achieve a speedy power-supply operation of the first and second driven circuits 21 and 22, it is necessary that the oscillation of the secondary oscillation part 135 becomes stable as quickly as possible after the start command signal is output to the control signal generating part 136 by the first driven circuit 21.

FIG. 5 shows a modification of the

secondary oscillation part 135 in the control circuit of FIG. 2. A secondary oscillation circuit 135' shown in FIG. 5 is provided in order to achieve a speedy power-supply operation of the first and second driven circuits 21 and 22. In FIG. 5, the elements which are essentially the same as corresponding elements in FIG. 2 are designated by the same reference numerals, and a description thereof will be omitted.

The secondary oscillation circuit 135' of FIG. 5 is constructed by a two-input AND gate and a PLL (phase-locked loop) circuit which are connected in a manner shown in FIG. 5. The AND gate has an input connected to an output of the control signal generating part 136, and an input connected to an output of the primary oscillation part 133. The AND gate has an output connected to an input of the PLL circuit. The PLL circuit has another input connected to an output of the secondary voltage detection part 130b. In response to a high-state clock signal output by the AND gate, the PLL circuit quickly produces a stable clock signal with a locked frequency, and supplies it to the second driven circuit 22.

In the secondary oscillation circuit 135' of FIG. 5, when the power-supply control signal at the output of the control signal generating part 136 is held

in a high state, the AND gate passing the clock signal, supplied by the primary oscillation part 133, to the PLL circuit. When a high-state clock signal output by the AND gate is received, the PLL circuit quickly produces a stable clock signal with the locked frequency, and supplies it to the second driven circuit 22. Hence, it is possible to achieve a speedy power-supply operation of the first and second driven circuits 21 and 22.

Further, in order to more effectively reduce the power consumption of the driven circuits, it is desirable to prevent the flow of a leak current from the first driven circuit 21 into the second driven circuit 22 when the supply of the secondary voltage to the second driven circuit 22 is stopped. When there is a difference in a drive voltage between the first driven circuit 21 and the second driven circuit 22, it is necessary to eliminate the voltage difference.

FIG. 6A and FIG. 6B show a modification of the first and second driven circuits 21 and 22 in the power control apparatus of FIG. 1.

In FIG. 6A, the first driven circuit 21 has inputs at which two-input AND gates 21a are provided, and the second driven circuit 22 has inputs at which buffer gates 22a are provided. Data signals output by the second driven circuit 22 are supplied to the AND gates 21a at the

inputs of the first driven circuit 21, and data signals output by the first driven circuit 21 are supplied to the buffer gates 22a at the inputs of the second driven circuit 22. In FIG. 6B, an example of the configuration of the respective inputs of the first and second driven circuits 21 and 22 is shown, in which one of the two-input AND gates 21a and one of the buffer gates 22a, shown in FIG. 6A, are constructed by MOS transistors and resistors which are connected in series as shown in FIG. 6B.

The first and second driven circuits 21 and 22 shown in FIG. 6A and FIG. 6B are provided to prevent the flow of a leak current from the first driven circuit 21 into the second driven circuit 22 when the supply of the secondary voltage to the second driven circuit 22 is stopped.

As shown in FIG. 6A, at the inputs of the first driven circuit 21, the two-input AND gates 21a are provided. Each AND gate 21a is constructed by a resistor and two MOS transistors. The resistor and the two MOS transistors are connected in series between a primary voltage line and a grounded base in a manner shown in FIG. 6B. Each AND gate 21a has an input (or a gate of one of the MOS transistors) connected to a signal line from the second driven circuit 22, and has an input (or a gate of the other MOS transistor) connected to an output (the

power-supply control signal) of the control signal generating part 136.

When the power-supply control signal at the output of the control signal generating part 136 is held in a high state, the AND gate 21a sets the first driven circuit 21 in an operating condition that it can receive a data signal supplied by the second driven circuit 22 via the signal line. When the data signal that is set in a high state by the second driven circuit 22 is received, the AND gate 21a of the first driven circuit 21 converts the received data into a high-state data signal based on the primary voltage.

As shown in FIG. 6A, at the inputs of the second driven circuit 22, the buffer gates 22a are provided. Each buffer gate 22a is constructed by a resistor and a MOS transistor. The resistor and the MOS transistor are connected in series between a secondary voltage line and a grounded base in a manner shown in FIG. 6B. Each buffer gate 22a has an input (or a gate of the MOS transistor) connected to a signal line from the first driven circuit 21, and has an output connected to an internal element (not shown) of the second driven circuit 22. When the data signal that is set in a high state by the first driven circuit 21 is received from the signal line, the buffer gate 22a of the second driven circuit 22

converts the received data into a high-state data signal based on the secondary voltage.

In the above-described embodiment of the power control apparatus in which the first and second driven circuits 21 and 22 of FIG. 6A and FIG. 6B are provided, it is possible to prevent the flow of a leak current from the MOS transistor of the first driven circuit 21 into the second driven circuit 22 when the supply of the secondary voltage to the second driven circuit 22 is stopped. Hence, it is possible to more effectively reduce the power consumption of the first and second driven circuits 21 and 22.

Further, the present invention is not limited to the above-described embodiments, and variations and modifications may be made without departing from the scope of the present invention.

The present invention is based on Japanese priority application No.10-067305, filed on March 17, 1998, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

1. A power control apparatus comprising:

a first driven circuit;

a second driven circuit connected to the first driven circuit;

a primary power-supply circuit for producing a primary voltage from a source voltage of a battery and supplying the primary voltage to drive the first driven circuit;

a secondary power-supply circuit for producing a secondary voltage from the source voltage of the battery or from the primary voltage of the primary power-supply circuit, and for supplying the secondary voltage to drive the second driven circuit; and

control means for outputting a power-supply control signal to the secondary power-supply circuit in response to a command signal, so that the supply of the secondary voltage to the second driven circuit by the secondary power-supply circuit is started or terminated by the power-supply control signal.

2. The apparatus according to claim 1, wherein the control means outputs a high-state power-supply control signal to the secondary power-supply circuit in response to a start command signal output by the first driven circuit, the high-state power-supply control signal causing the secondary power-supply circuit to start the supply of the secondary voltage to the second driven circuit.

3. The apparatus according to claim 1, wherein the control means outputs a low-state power-supply control signal to the secondary power-supply circuit in response to an end command signal output by the first driven circuit, the low-state power-supply control signal causing the secondary power-supply circuit to terminate the supply of the secondary voltage to the second driven circuit.

4. A power control apparatus comprising:

a first driven circuit;

a second driven circuit connected to the first driven circuit;

a primary power-supply circuit connected to a battery, the primary power-supply circuit producing a primary voltage from a source voltage of the battery and supplying the primary voltage to drive the first driven circuit;

a secondary power-supply circuit connected to the primary power-supply circuit, the secondary power-supply circuit producing a secondary voltage from the source voltage of the battery or from the primary voltage of the primary power-supply circuit and supplying the secondary voltage to drive the second driven circuit;

a primary oscillation part for outputting a clock signal to the first driven circuit;

a primary reset generating part for outputting a primary reset signal to the first driven circuit when an oscillation of the primary oscillation part is detected to be stable, the primary reset signal causing the first driven circuit to start operation in accordance with the clock signal output by the primary oscillation part;

a control signal generating part, connected to both the first driven circuit and the secondary power-

supply circuit, for outputting a power-supply control signal to the secondary power-supply circuit in response to a command signal output by the first driven circuit, so that the supply of the secondary voltage to the second driven circuit by the secondary power-supply circuit is started or terminated by the power-supply control signal;

a secondary oscillation part for outputting a clock signal to the second driven circuit; and

a secondary reset generating part for outputting a secondary reset signal to the second driven circuit when an oscillation of the secondary oscillation part is detected to be stable, the secondary reset signal causing the second driven circuit to start operation in accordance with the clock signal output by the secondary oscillation part.

5. The apparatus according to claim 4, wherein the secondary oscillation part includes a gate circuit and a phase-locked loop PLL circuit, the gate circuit having a first input connected to an output of the control signal generating part, a second input connected to an output of the primary oscillation part, and an

output connected to an input of the PLL circuit, the gate circuit passing the clock signal from the primary oscillation part to the PLL circuit when a high-state power-supply control signal is received at the first input, the PLL circuit producing a clock signal with a locked frequency when a high-state clock signal output by the gate circuit is received, and supplying the clock signal to the second driven circuit.

6. The apparatus according to claim 4, wherein the second driven circuit includes a buffer gate at an input of the second driven circuit, the input of the second driven circuit being connected to an output of the first driven circuit via a signal line, the buffer gate, when a data signal set in a high state by the first driven circuit is received from the signal line, converting the received data into a high-state data signal based on the secondary voltage.

7. The apparatus according to claim 6, wherein the buffer gate includes a resistor and a metal-oxide-semiconductor transistor connected in series between a secondary voltage line and a grounded base.

8. The apparatus according to claim 4, wherein the first driven circuit includes a gate circuit at an input of the first driven circuit, the input of the first driven circuit being connected to an output of the second driven circuit via a signal line, the gate circuit having a first input connected to the signal line and a second input connected to an output of the control signal generating part, the gate circuit enabling the first driven circuit to receive a data signal from the signal line when a high-state power-supply control signal output by the control signal generating part is received at the second input, and when the data signal that is set in a high state by the second driven circuit is received, the gate circuit converting the received data into a high-state data signal based on the primary voltage.

9. The apparatus according to claim 8, wherein the gate circuit includes a resistor and two metal-oxide-semiconductor transistors connected in series between a primary voltage line and a grounded base.

10. The apparatus according to claim 4, wherein the control signal generating part outputs a high-state power-supply control signal to the secondary power-supply circuit in response to a start command signal output by the first driven circuit, the high-state power-supply control signal causing the secondary power-supply circuit to start the supply of the secondary voltage to the second driven circuit.

11. The apparatus according to claim 4, wherein the control signal generating part outputs a low-state power-supply control signal to the secondary power-supply circuit in response to an end command signal output by the first driven circuit, the low-state power-supply

control signal causing the secondary power-supply circuit to terminate the supply of the secondary voltage to the second driven circuit.

ABSTRACT OF THE DISCLOSURE

A power control apparatus includes a first driven circuit and a second driven circuit connected to the first driven circuit. A primary power-supply circuit produces a primary voltage from a source voltage of a battery and supplies the primary voltage to drive the first driven circuit. A secondary power-supply circuit produces a secondary voltage from the source voltage of the battery or from the primary voltage of the primary power-supply circuit, and supplies the secondary voltage to drive the second driven circuit. A control circuit outputs a power-supply control signal to the secondary power-supply circuit in response to a command signal, so that the supply of the secondary voltage to the second driven circuit by the secondary power-supply circuit is started or terminated by the power-supply control signal.

FIG.1

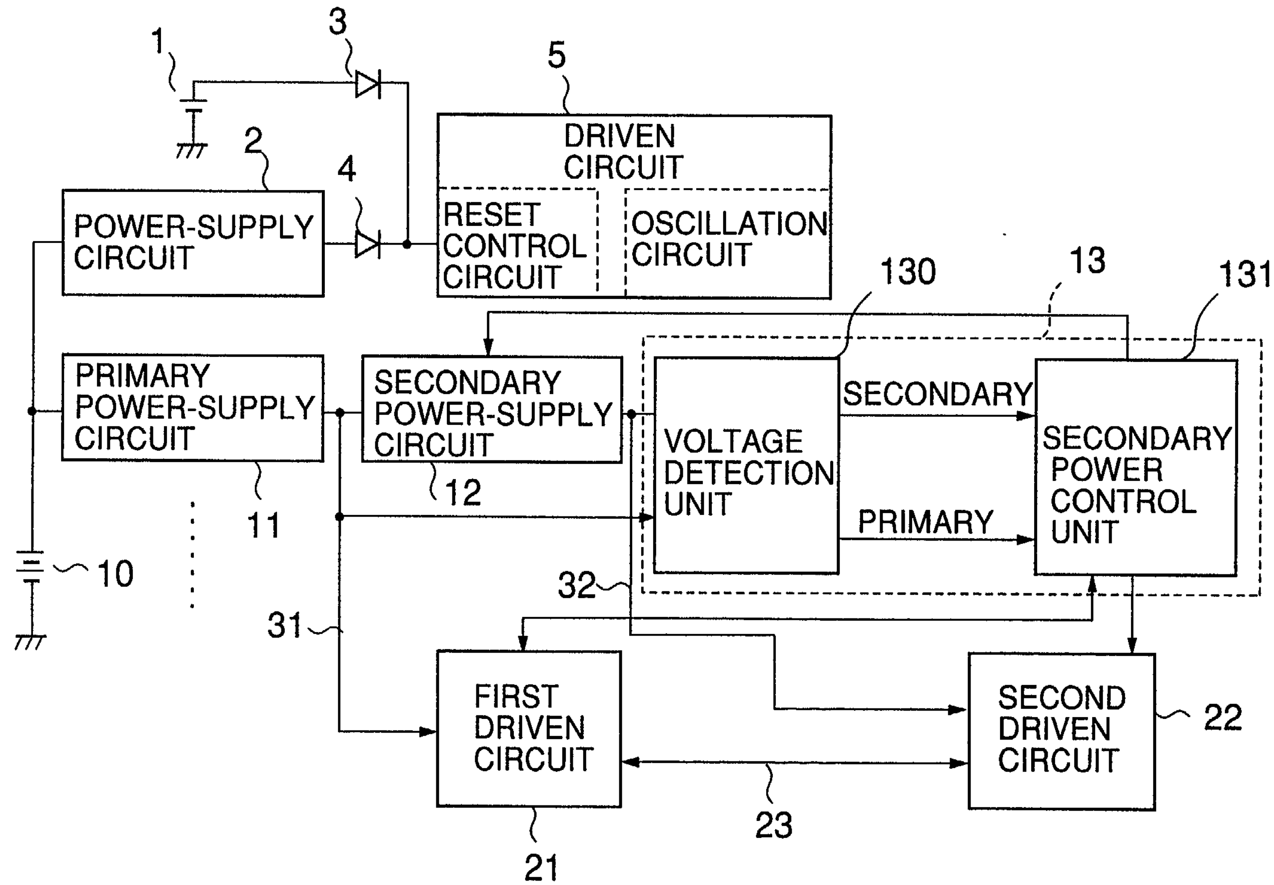

1
2
3
4
5
POWER-SUPPLY CIRCUIT
DRIVEN CIRCUIT
RESET CONTROL CIRCUIT
OSCILLATION CIRCUIT
PRIMARY POWER-SUPPLY CIRCUIT
SECONDARY POWER-SUPPLY CIRCUIT
VOLTAGE DETECTION UNIT
SECONDARY
PRIMARY
SECONDARY POWER CONTROL UNIT
130
13
131
11
12
10
31
32
FIRST DRIVEN CIRCUIT
SECOND DRIVEN CIRCUIT
21
22
23

FIG.2

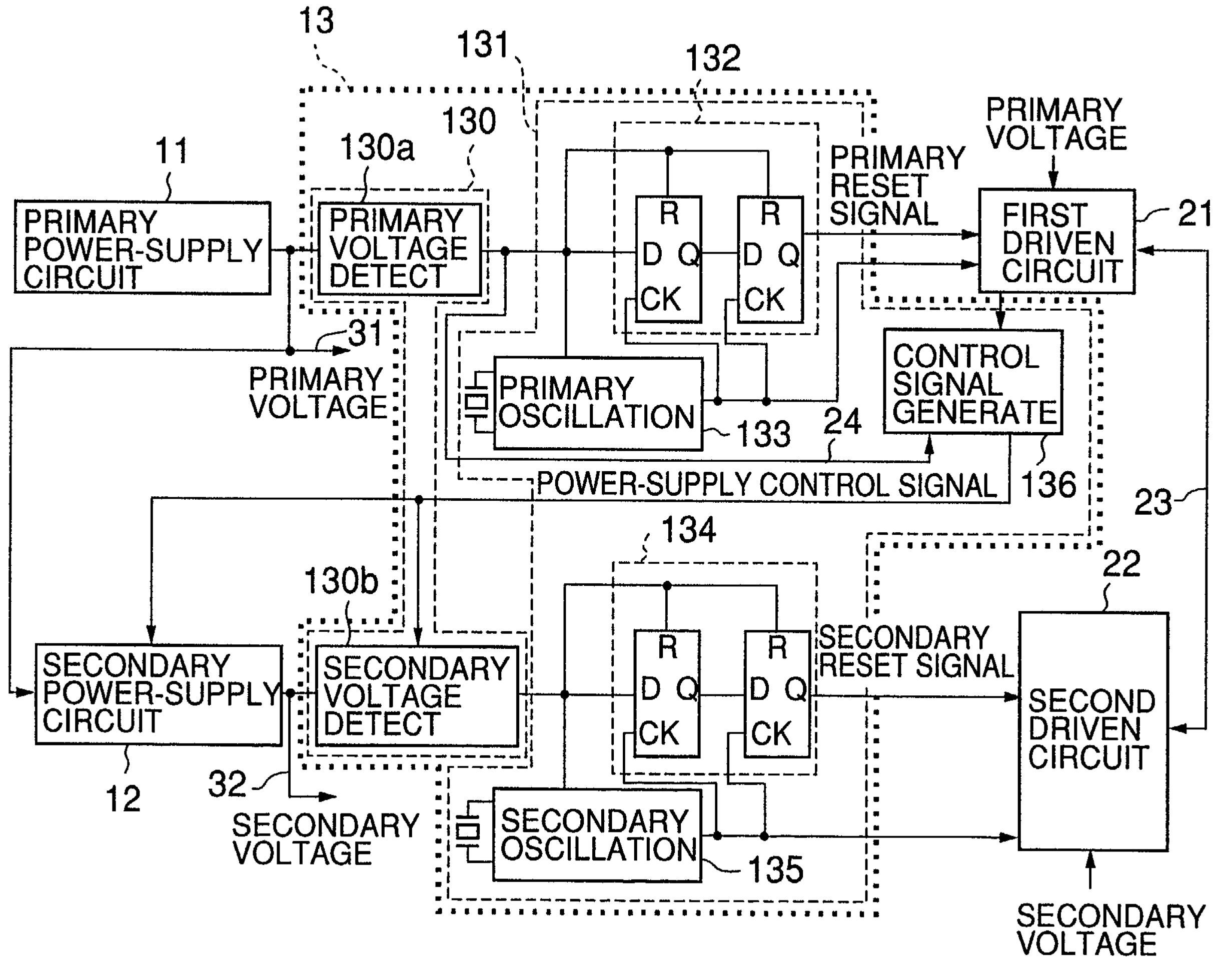

13
131
132
130a
130
11
PRIMARY POWER-SUPPLY CIRCUIT
PRIMARY VOLTAGE DETECT
R
D Q
CK
R
D Q
CK
PRIMARY RESET SIGNAL
PRIMARY VOLTAGE
FIRST DRIVEN CIRCUIT
21
31
PRIMARY VOLTAGE
PRIMARY OSCILLATION
133
24
CONTROL SIGNAL GENERATE
136
POWER-SUPPLY CONTROL SIGNAL
23
134
130b
22
SECONDARY POWER-SUPPLY CIRCUIT
SECONDARY VOLTAGE DETECT
SECONDARY RESET SIGNAL
SECOND DRIVEN CIRCUIT
12
32
SECONDARY VOLTAGE
SECONDARY OSCILLATION
135
SECONDARY VOLTAGE

FIG.3

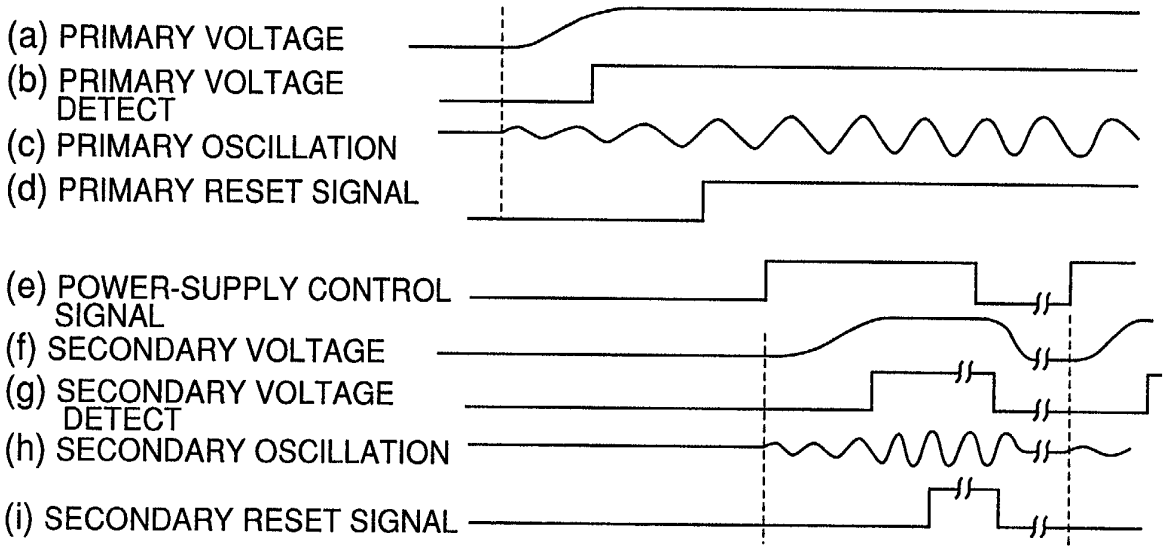

(a) PRIMARY VOLTAGE
(b) PRIMARY VOLTAGE DETECT
(c) PRIMARY OSCILLATION
(d) PRIMARY RESET SIGNAL
(e) POWER-SUPPLY CONTROL SIGNAL
(f) SECONDARY VOLTAGE
(g) SECONDARY VOLTAGE DETECT
(h) SECONDARY OSCILLATION
(i) SECONDARY RESET SIGNAL

FIG.4

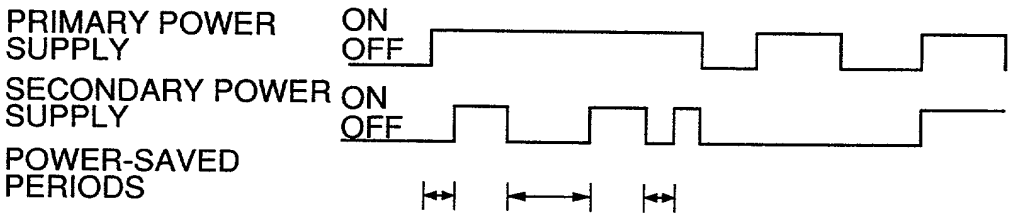

PRIMARY POWER SUPPLY
ON
OFF
SECONDARY POWER SUPPLY
ON
OFF
POWER-SAVED PERIODS

FIG.5

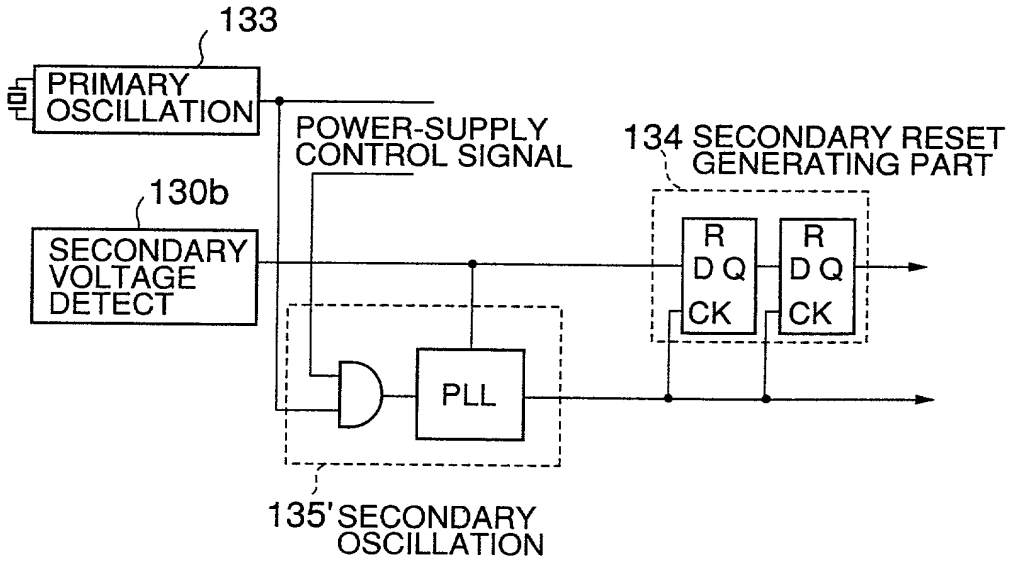

133
PRIMARY OSCILLATION
POWER-SUPPLY CONTROL SIGNAL
134 SECONDARY RESET GENERATING PART
130b
SECONDARY VOLTAGE DETECT
R
D Q
CK
R
D Q
CK
PLL
135' SECONDARY OSCILLATION

FIG.6A

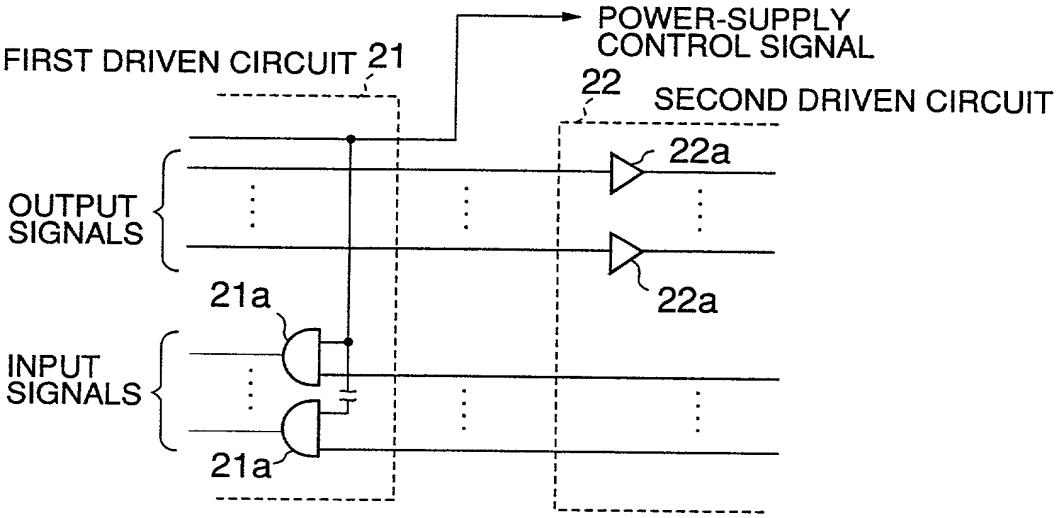

POWER-SUPPLY
CONTROL SIGNAL
FIRST DRIVEN CIRCUIT 21
22
SECOND DRIVEN CIRCUIT
22a
OUTPUT
SIGNALS
22a
21a
INPUT
SIGNALS
21a

FIG.6B

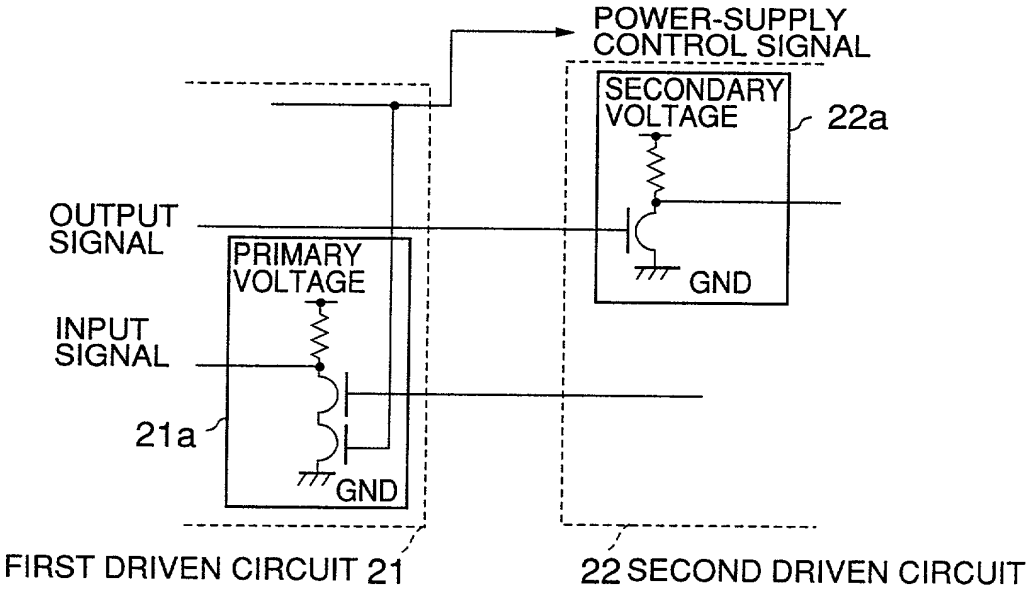
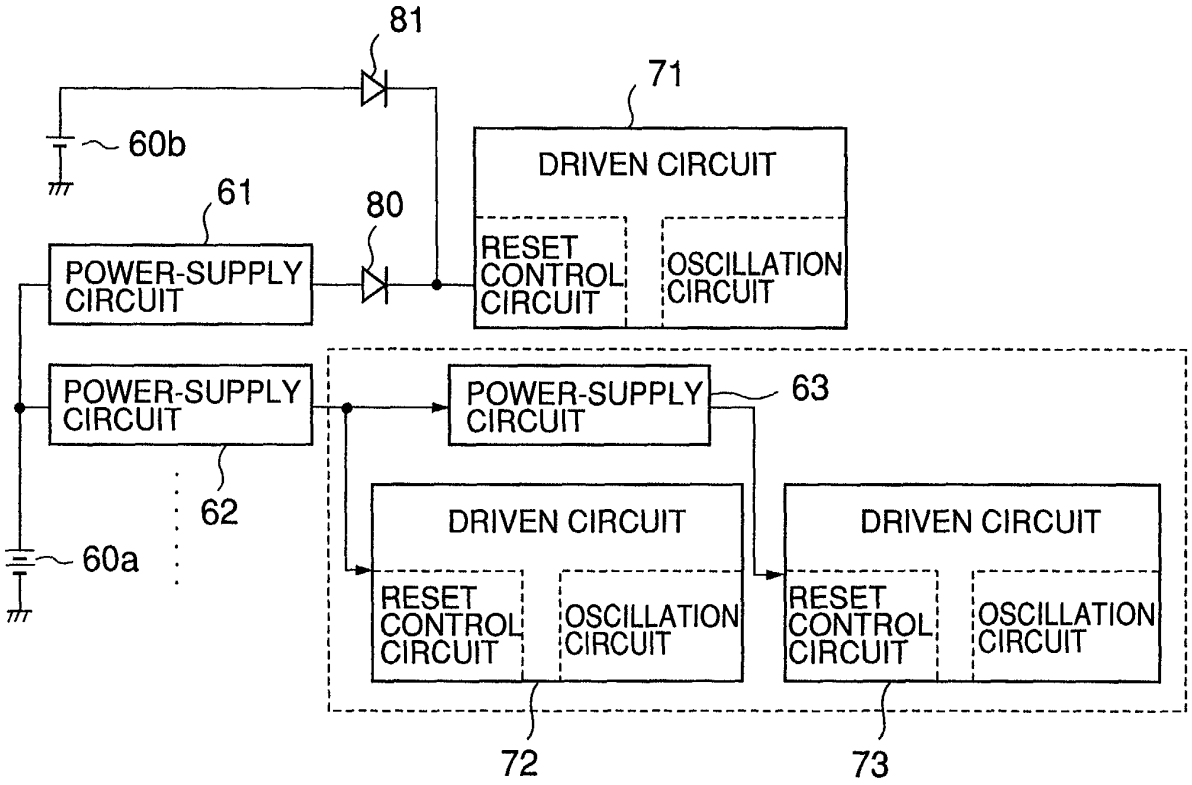

POWER-SUPPLY
CONTROL SIGNAL
SECONDARY
VOLTAGE
22a
OUTPUT
SIGNAL
PRIMARY
VOLTAGE
GND
INPUT
SIGNAL
21a
GND
FIRST DRIVEN CIRCUIT 21
22 SECOND DRIVEN CIRCUIT

FIG.7 PRIOR ART



Docket No.
R2184.045/P045

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

POWER CONTROL APPARATUS FOR A BATTERY-POWERED COMMUNICATION SYSTEM

the specification of which

(check one)

[X] is attached hereto.

[ ] was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
Patent Application No. 10-067305	Japan	17/March/1998	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; Juliana Haydoutova, P43,313; James M. Heintz, P41,828; Herbert V. Kerner, P42,721; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M. Silbermann, 40,413; Richard Veltman, 36,957 and Darius Gambino, 41,472.

Send Correspondence to:

Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, N.W.
Washington, D.C. 20037-1526

Direct Telephone Calls to:

202-785-9700

Full name of sole or first inventor TATSUYA FUJII
Sole or first inventor's signature — Date Tatsuya Fujii — February 2, 1999
Residence Kanagawa, Japan
Citizenship Japan
Post Office Address c/o RICOH COMPANY, LTD., 3-6, Nakamagome 1-chome, Ohta-ku, Tokyo 143-8555, Japan

Full name of second inventor, if any
Second inventor's signature — Date
Residence
Citizenship
Post Office Address